

AC Controlling Thyristor, 30A

FEATURES

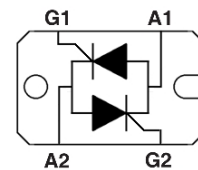
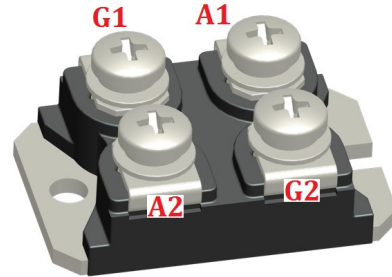
- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Advance power cycling
- UL approved file E320098
- Compliant to RoHS

APPLICATIONS

- Line rectifying 50/60Hz
- DC Motor control
- Softstart AC motor control
- AC power control
- Power converter
- Light and temperature control

PACKAGE (SOT-227)

- Isolation voltage:3000V
- Industry standard outline
- Epoxy meets UL 94V-0
- Copper base plate, internally DCB isolated



PRODUCT SUMMARY

$I_{T(AV)}$	30A
V_{DRM}/V_{RRM}	1200~1600 V
I_{GT}	20~100 mA

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	TEST CONDITIONS		VALUE	UNIT
Maximum RMS on-state current	$I_{T(RMS)}$	180° conduction half sine wave, 50Hz	$T_C = 95^\circ C$	47	A
Maximum average on-state current	$I_{T(AV)}$	180° conduction half sine wave, 50Hz	$T_C = 95^\circ C$	30	A
Maximum non-repetitive peak on-state surge current (full cycle, T_J initial = 25°C)	I_{TSM}	F = 50 Hz	t = 20 ms	500	A
		F = 60 Hz	t = 16.7 ms	525	
Maximum I^2t Value for fusing	I^2t	$t_p = 10$ ms		1250	A ² s
Critical rate of rise of on-state current	di/dt	$V_D = 67\% V_{DRM}$, $t_p = 200\mu s$, $I_G = 0.3A$ $di_G/dt = 0.3A/\mu s$, F = 50 Hz	$T_J = 150^\circ C$	100	A/ μs
Peak gate current	I_{GM}	$T_p = 20 \mu s$	$T_J = 150^\circ C$	3	A
Maximum gate power	P_{GM}	$T_p = 20\mu s$	$T_J = 150^\circ C$	10	W
Average gate power dissipation	$P_{G(AV)}$	$T_J = 150^\circ C$		3	W
Repetitive peak off-state voltage	V_{DRM}	$T_J = 150^\circ C$		1200~1600	V
Repetitive peak reverse voltage	V_{RRM}				
Maximum power dissipation	P_D		$T_C = 25^\circ C$	139	W
Storage temperature range	T_{stg}			- 40 to + 150	°C
Maximum junction temperature range	T_J			- 40 to + 150	
Maximum operation temperature	T_{OP}			- 40 to + 125	

ELECTRICAL SPECIFICATIONS (T_J = 25 °C unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		Value			Unit
				Min.	Typ.	Max.	
Gate trigger current	I _{GT}	V _D = 6V, R _L = 30Ω		20	-	100	mA
Gate trigger voltage	V _{GT}			-	-	1.4	V
Gate non-trigger voltage	V _{GD}	V _D = ⅔ V _{DRM}	T _J = 150°C	-	-	0.25	V
Gate non-trigger current	I _{GD}	V _D = ⅔ V _{DRM}	T _J = 150°C	-	-	10	mA
Holding current	I _H	I _T = 1A, Gate open		-	-	150	mA
Latching current	I _L	I _G = 1.2 x I _{GT}		-	-	250	mA
Critical rate of rise of voltage	dv/dt	V _D = ⅔ V _{DRM} , Gate open	T _J = 150°C	-	-	1000	V/μs
Forward voltage drop	V _{TM}	I _T = 30A, t _p = 380μs	T _J = 25°C	-	-	1.30	V
Off-state and reverse leakage current	I _{DRM} I _{RRM}	V _D =V _{DRM} , V _R =V _{RRM}	T _J = 25°C	-	-	20	μA
			T _J = 150°C	-	-	5	mA
RMS isolation voltage	V _{ISO}	50Hz, circuit to base, all terminals shorted, I _{ISO} ≤ 1mA	t = 1 min	2500	-	-	V
			t = 1 s	3000	-	-	
Maximum threshold voltage	V _{T(TO)}		T _J = 150°C	-	-	0.90	V
Maximum slope resistance	r _T		T _J = 150°C	-	-	13.5	mΩ

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUE	UNIT
Maximum thermal resistance, junction to case	R _{thJC}	DC operation	0.90	°C/W
Typical thermal resistance, case to heatsink	R _{thCS}	Mounting surface flat, smooth and greased	0.10	°C/W
Mounting force, ±10% to heatsink, M4 busbar, M4		A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound	1.1	N.m
			1.1	
Approximate weight			30	g
			1.06	oz.
Case style		JEDEC	SOT-227	

ORDERING INFORMATION SCHEME

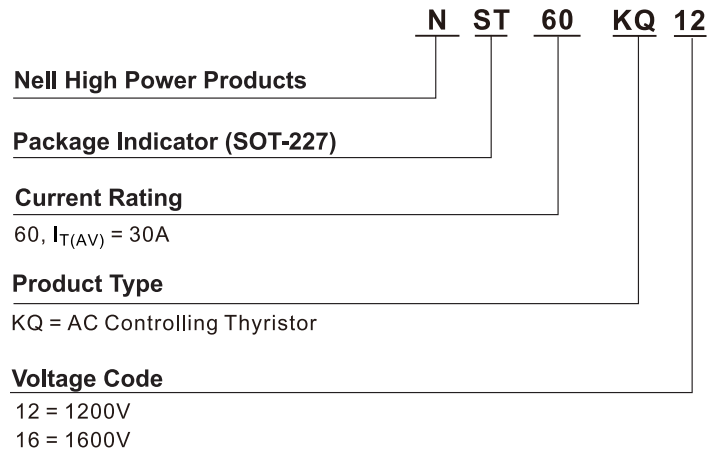


Fig.1 Peak on-state voltage vs. peak on-state current

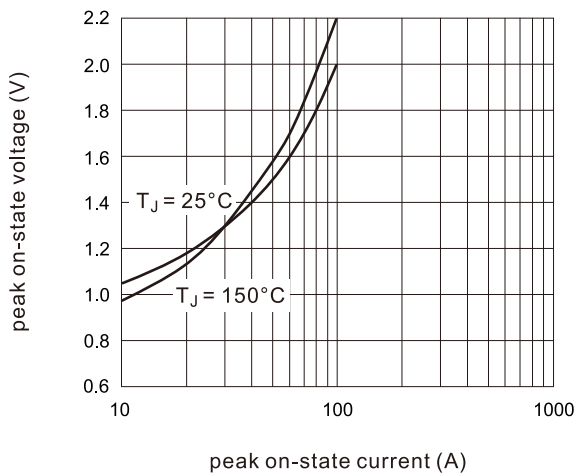


Fig.2 Max. junction to case thermal Impedance vs. time

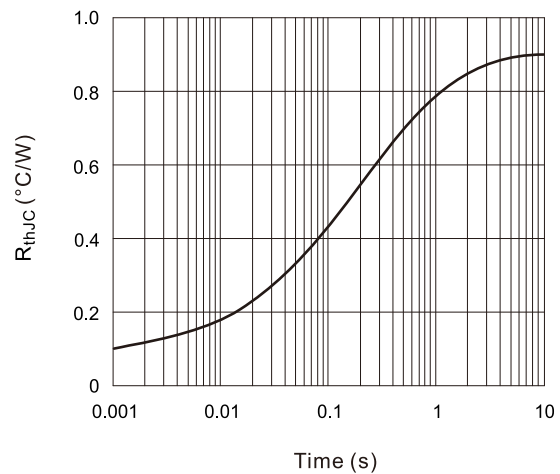


Fig.3 Power dissipation vs. average on-state current

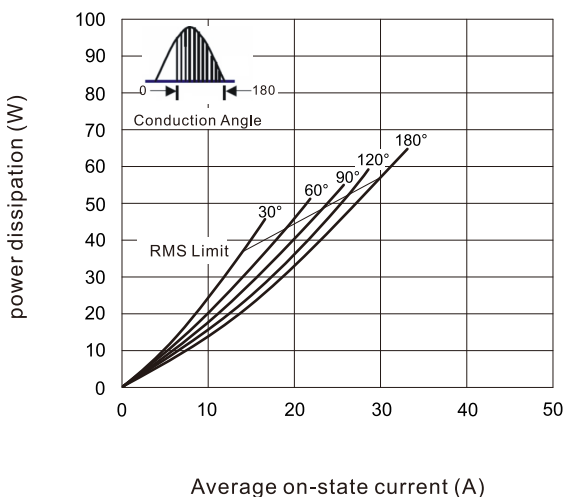


Fig.4 Case Temperature Vs. Average On-state Current

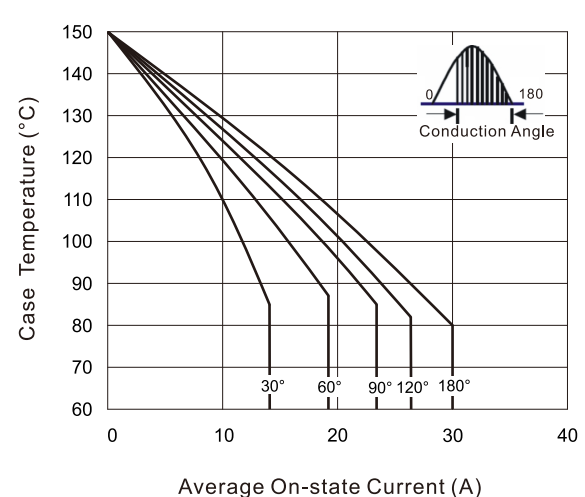


Fig.5 Surge on-state current vs. cycles

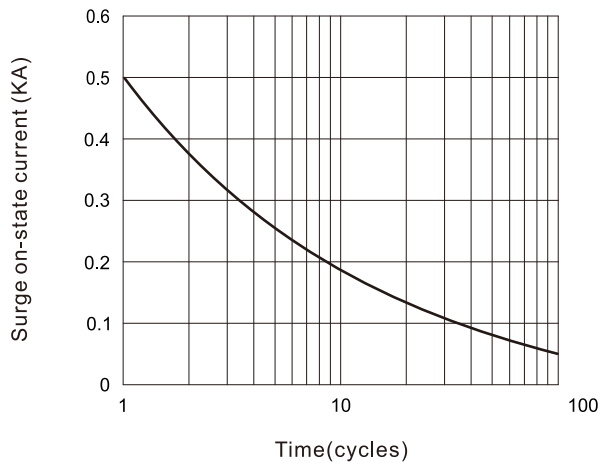
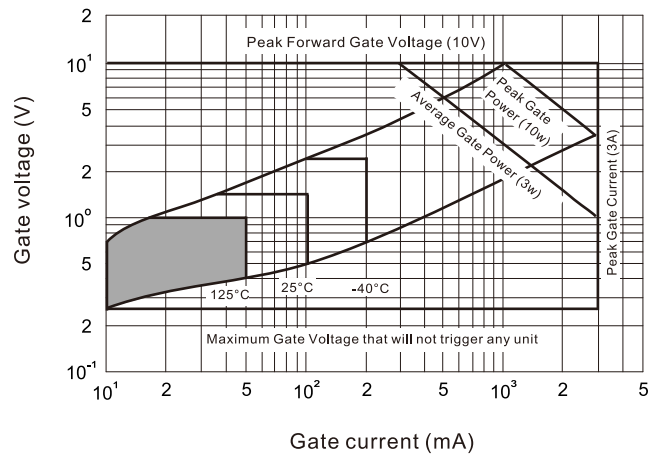
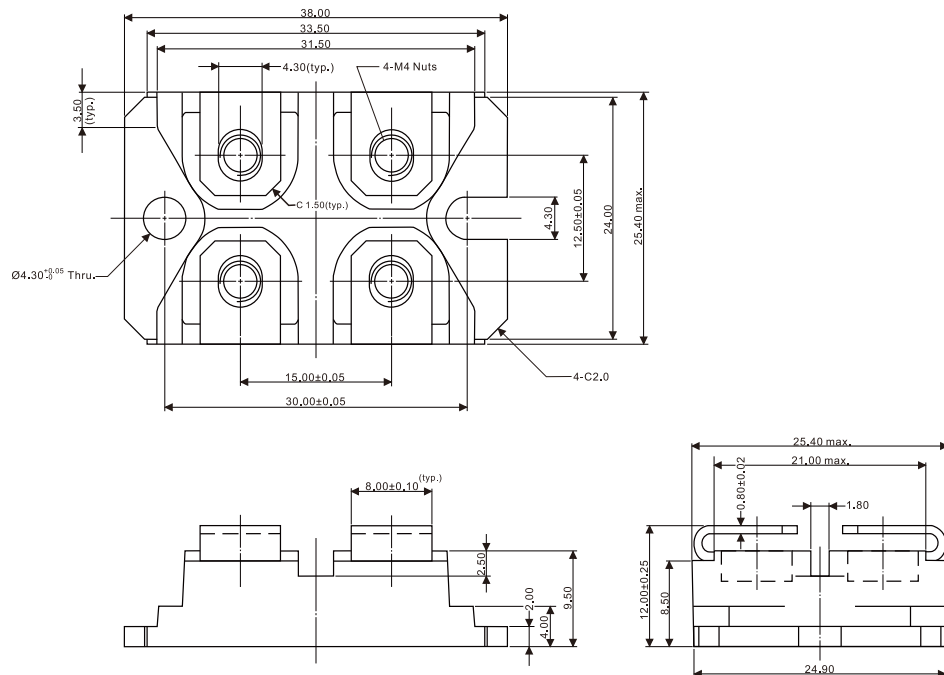


Fig.6 Gate characteristics



Case Style

SOT-227



All dimensions in millimeters